30th International Workshop on Logic & Synthesis

July 19 – 22, 2021

Virtual Conference

IWLS 2021 Proceedings

Please find the IWLS 2021 proceedings here

IWLS 2021 Technical Program

	PT	JST	CEST
Day 1	**Monday, July 19, 8:50am - 2:00pm**	Tuesday, July 20, 0:50am - 6:00am	Monday, July 19, 5:50pm - 11:00pm
Day 2	Tuesday, July 20, 5:00 pm - 8:55 pm	**Wednesday, July 21, 9:00am - 1:55pm**	Wednesday, July 21, 2:00am - 5:55am
Day 3	Thursday, July 22, 0:00am - 3:40 am	Thursday, July 22, 4:00pm - 7:40pm	**Thursday, July 22, 9:00am - 12:40pm**

Monday July 19 based in Pacific Time (PT)

08:50 - 9:00am (PT) / 12:50 - 1:00am (JST) / 5:50 - 6:00pm (CEST):
Workshop Opening
Vinicius Callegaro, Cunxi Yu, and Gai Liu
Record @Youtube

9:00 - 10:00am (PT) / 1:00 - 2:00am (JST) / 6:00 - 7:00pm (CEST):
Keynote 1: QED and Symbolic QED: Dramatic Advances in Hardware Verification, Debug, and Security.
Subhasish Mitra, Stanford, United States
Session Chair: Luca Amaru, Synopsys
Record @Youtube

10:00 - 10:15am (PT) / 2:00 - 2:15am (JST) / 7:00 - 7:15pm (CEST):
Break

10:15am - 11:25am (PT) / 2:15 - 3:25am (JST) / 7:15 - 8:25pm (CEST):
Session 1: Logic Synthesis & Optimization
Session Chair: Alan Mishchenko, UC Berkeley
Record @Youtube

Boolean Rewriting Strikes Back: Reconvergence-Driven Windowing Meets Resynthesis
Heinz Riener (*EPFL, Switzerland*), Siang-Yun Lee (*EPFL, Switzerland*), Alan Mishchenko (*UC Berkeley, USA*) and Giovanni De Micheli (*EPFL, Switzerland*)
Talk @Youtube

From Logic to Gates: A Versatile Mapping Approach to Restructure Logic
Alessandro Tempia Calvino (*EPFL, Switzerland*), Heinz Riener (*EPFL, Switzerland*), Shubham Rai (*TU Dresden, Germany*) and Giovanni De Micheli (*EPFL, Switzerland*)
Talk @Youtube

Structure Aware Partitioning for Mixed Logic Synthesis
Ashton Snelgrove, Scott Temple and Pierre-Emmanuel Gaillardon (*University of Utah, USA*)
Talk @Youtube

Exploring Logic Gates Susceptibility and Circuit Mapping in Reliability Analysis (Short Presentation)
Matheus Pontes (*UFPEL, Brazil*), Rafael Schvittz (*FURG, Brazil*), Leomar S. Rosa Junior (*UFPEL, Brazil*) and Paulo F. Butzen

(*UFRGS, Brazil*)
Talk @Youtube

11:25 - 11:40am (PT) / 3:25 - 3:40am (JST) / 8:25 - 8:40pm (CEST):
Break

11:40 - 12:30pm (PT) / 3:40 - 4:30am (JST) / 8:40 - 9:30pm (CEST):
Programming Contest: Presentation and Results
Session Chairs: Alan Mishchenko (*UC Berkeley, USA*), Sat Chatterjee (*Google, USA*), and Gai Liu (*Xilinx, USA*)
Presentation slides
Record @Youtube

1st team presentation: University of Wisconsin–Madison
Talk @Youtube

2nd team presentation: National Taiwan University
Talk @Youtube

3rd team presentation: UC Berkeley + U Tokyo + IIT KGP + IIT B
Talk @Youtube

12:30 - 12:45pm (PT) / 4:30 - 4:45am (JST) / 9:30 - 9:45pm (CEST):
Break

12:45 - 2:00pm (PT) / 4:45 - 6:00am (JST) / 9:45 - 11:00pm (CEST):
Special Session: Machine Learning for Logic Synthesis and Vice-Versa
Session Chair: Cunxi Yu, University of Utah
Record @Youtube

Talk 1: Nanosecond Inference Engines for Particle Detectors
Claudionor Coelho (*Palo Alto Networks, USA*) and Thea Klaeboe Aarrestad (*CERN, CH*)

Talk 2: Learning-based Techniques for Automatic Logic Optimization.
Pierre-Emmanuel Gaillardon (*University of Utah, USA*)

Talk 3: Logic Synthesis for Hardware Accelerators
Alan Mishchenko (*UC Berkeley, USA*)

Wednesday July 21 based in Japan Standard Time (JST)

5:00 - 6:00pm (PT) / **9:00 - 10:00am (JST)** / 2:00 - 3:00am (CEST):
Keynote 2: Circuit Learning: A Classical Problem from a Modern Perspective.
Jie-Hong Roland Jiang, NTU, Taiwan
Session Chair: Vinicius Callegaro,Siemens EDA, USA
Record @Youtube

6:00 - 6:15pm (PT) / **10:00 - 10:15am (JST)** / 3:00 - 3:15am (CEST):
Break

6:15 - 7:25pm (PT) / **10:15 - 11:25am (JST)** / 3:15 - 4:25am (CEST):
Session 2: Approximation and Correctness of Logic Design
Session Chair: Gai Liu, Xilinx
Record @Youtube

RUCA: RUntime Configurable Approximate Circuits with Self-Correcting Capability
Jingxiao Ma and Sherief Reda (*Brown University, USA*)
Talk @Youtube

A method to join the On-set and Off-set of an incompletely boolean function into a single BDD
Renato D. Peralta, João P. Nespolo, Paulo F. Butzen, Mariana L. Kolberg and André I. Reis (*UFRGS, Brazil*)
Talk @Youtube

On the Rectification of Finite Field Arithmetic Circuits Using Computer Algebra Techniques
Vikas Rao (*University of Utah, USA*), Haden Ondricek (*University of Utah, USA*), Priyank Kalla (*University of Utah, USA*) and Florian Enescu (*Georgia State University, USA*)
Talk @Youtube

Two-Level Approximate Logic Synthesis (Short Presentation)
Gabriel Ammes (*UFRGS, Brazil*), Walter Lau Neto (*University of Utah, USA*), Paulo F. Butzen (*UFRGS, Brazil*), Pierre-Emmanuel Gaillardon (*University of Utah, USA*) and Renato Ribas (*UFRGS, Brazil*)
Talk @Youtube

7:25 - 7:40pm (PT) / **11:25 - 11:40am (JST)** / 4:25 - 4:40am (CEST):
Break

7:40 - 8:40pm (PT) / **11:40 - 12:40pm (JST)** / 4:40 - 5:40am (CEST):
Session 3: When Synthesis Meets Machine Learning
Session Chair: Walter Lau Neto, University of Utah
Record @Youtube

On A Design of Multi-Layer LUT Networks
Tsutomu Sasao (*Meiji University, Japan*)
Talk @Youtube

Henkin Synthesis: DQBF meets Machine Learning
Priyanka Golia (*IIT Kanpur, India*), Subhajit Roy (*IIT Kanpur, India*) and Kuldeep S. Meel (*National University of Singapure, Singapure*)
Talk @Youtube

Two Methods Based on AIG Constant Propagation to Reduce Neural Network Circuits (Short Presentation)
Augusto Berndt (*UFSC, Brazil*), Cristina Meinhardt (*UFSC, Brazil*), Andre Reis (*UFRGS, Brazil*) and Paulo F. Butzen (*UFRGS, Brazil*)
Talk @Youtube

Unit Time Modelling of Asynchronous and Pulse-Gate Circuits (Short Presentation)
David McCarthy (UC Santa Barbara, USA) and Forrest Brewer (UC Santa Barbara, USA)
Talk @Youtube

8:40 - 8:55pm (PT) / **12:40 - 12:55pm (JST)** / 5:40 - 5:55am (CEST):
Break

8:55 - 9:55pm (PT) / **12:55 - 1:55pm (JST)** / 5:55 - 6:55am (CEST):
Session 4: Machine Learning for Logic Synthesis
Session Chair: Jody Matos, Sivaco
Record @Youtube

A Supervised Learning Approach for Technology Mapping
Walter Lau Neto (*University of Utah, USA*) , Matheus Trevisan Moreira (*Chronos Tech, USA*), Yingjie Li (*University of Utah, USA*), Luca Amaru (*Synopsys Inc., USA*), Cunxi Yu (*University of Utah, USA*) and Pierre-Emmanuel Gaillardon (*University of Utah, USA*)
Talk @Youtube

Quantized Neural Network Synthesis for Direct Logic Circuit Implementation
Yu-Shan Huang (*National Taiwan University, Taiwan*), Jie-Hong Roland Jiang (*National Taiwan University, Taiwan*) and Alan Mishchenko (*UC Berkeley, USA*)
Talk @Youtube

RL-Guided Runtime-Constrained Heuristic Exploration for Logic Synthesis
Yasasvi V. Peruvemba (*IIT Indore, India*), Shubham Rai (*TU Dresden, Germany*), Kapil Ahuja (*IIT Indore, India*) and Akash Kumar (*TU Dresden, Germany*)
Talk @Youtube

Thursday July 22 based in Central European Summer Time

12:00 - 1:00am (PT) / 4:00 - 5:00pm (JST) / **9:00 - 10:00am (CEST)**:
Keynote 3: Superconducting accelerators: circuits, design and synthesis.
Giovanni De Micheli, EPFL, Switzerland
Session Chair: Mathias Soeken, Microsoft
Record @Youtube

1:00 - 1:15am (PT) / 5:00 - 5:15pm (JST) / **10:00 - 10:15am (CEST)**:
Break

1:15 - 2:25am (PT) / 5:15 - 6:25pm (JST) / **10:15 - 11:15am (CEST)**:
Session 5: Physical Synthesis and Synthesis for Emerging Technologies
Session Chair: Weikang Qian, Shanghai Jiao Tong University
Record @Youtube

Irredundant Buffer and Splitter Insertion and Scheduling-Based Optimization for AQFP Circuits
Siang-Yun Lee, Heinz Riener and Giovanni De Michel (*EPFL, Switzerland*)
Talk @Youtube
Talk @bilibili

Constraint-based hierarchical placement for FPGAs
Yukio Miyasaka, Alan Mishchenko and John Wawrzynek (*UC Berkeley, USA*)
Talk @Youtube
Talk @bilibili

Linear Feedback Shift Register Reseeding for Stochastic Circuit Repairing and Minimization
Chen Wang and Weikang Qian (*Shanghai Jiao Tong University, China*)
Talk @Youtube
Talk @bilibili

Optimizing Adiabatic Quantum-Flux-Parametron (AQFP) Circuits using Exact Methods (Short Presentation)
Dewmini Sudara Marakkalage, Heinz Riener and Giovanni De Micheli (*EPFL, Switzerland*)
Talk @Youtube
Talk @bilibili

2:25 - 2:35am (PT) / 6:25 - 6:35pm (JST) / **11:25 - 11:35am (CEST)**:
EPFL Benchmark Results Update
Alessandro Tempia Calvino, Heinz Riene (EPFL, Swtizerland)
Record @Youtube

2:35 - 2:40am (PT) / 6:35 - 6:40pm (JST) / **11:35 - 11:40am (CEST)**:
Break

2:40 - 3:40am (PT) / 6:40 - 7:40pm (JST) / **11:40 - 12:40pm (CEST)**:
Session 6: Formal Methods and Applications
Session Chair: Eleonora Testa, Synopsys
Record @Youtube

A Circuit-Based SAT Solver for Logic Synthesis
He-Teng Zhang (*National Taiwan University, Taiwan*), Jie-Hong Jiang (*National Taiwan University, Taiwan*) and Alan Mishchenko (*UC Berkeley, USA*)
Talk @Youtube

Compatible Equivalence Checking of X-Valued Circuits
Yu-Neng Wang, Yun-Rong Luo, Po-Chun Chien, Ping-Lun Wang, Hao-Ren Wang, Wan-Hsuan Lin, Jie-Hong Roland Jiang and Chung-Yang Ric Huang (*National Taiwan University, Taiwan*)
Talk @Youtube

Polynomial Formal Verification of Prefix Adders
Alireza Mahzoon and Rolf Drechsler (*University of Bremen, Germany*)
Talk @Youtube

Request a certificate

IWLS'21 will provide certificates for attendees and speakers. You can request a certificate **here**.
Please notice: attendance will be cross-checked with the Zoom participant entry list.